

Radiation Tolerant Intelligent Memory Stack (RTIMS)

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- Introduction
- Development
- Radiation Mitigation
- Environmental Testing



The Reasons:

- NASA has identified many systems that will require onboard data processing for future missions.
- These missions will require increased resolution, improved data quality, and additional capacity for raw and/or processed data.
- The requirement to efficiently handle large data sets necessitates the use of larger, faster on-board memories.

In this presentation we will discuss the development and test of a radiation tolerant memory, suitable for both geostationary (GEO) and low earth orbit (LEO) missions.



The Requirements:

- Large memory array
- Compact packaging
- Radiation Tolerance
- Rugged
- Reprogrammable



What We Built:

- A large memory array
 - 2 Gigabits EDAC or 1 Gigabit TMR
- Compact packaging
 - 42.7mm x 42.7mm x 13.00mm
 - 60 grams
- Radiation Tolerance
 - 100Krad (SI) TID
 - 60MeV -cm²/mg at 25°C Latch-up Immune
- Rugged
 - -40°C/+85°C Operating (Vacuum 10⁻⁵ torr)
 - 10.0 Grms vibration over 20 to 2000 Hz
 - 1000 hours life test
- Reprogrammable
 - Xilinx based controller



Radiation Tolerant Intelligent Memory Stack (RTIMS)

PI: Jeffrey A. Herath, NASA Langley Research Center

Description and Objectives

Description:

A radiation tolerant memory, suitable for both geo-stationary and low earth orbit missions, which provides 2 gigabits of error corrected digital memory. By using FPGA technology, RTIMS will also be a key element in adaptive/reconfigurable computing applications. RTIMS will significantly enhance a broad range of high data rate missions.

Objectives:

- •Develop a radiation tolerant memory component, suitable for GEO, LEO and MEO missions, which provides 2 gigabits of error corrected memory space using new stacking and radiation shielding technologies.
- •Design, test and integrate the Radiation Tolerant Intelligent Memory Stack (RTIMS) onto a 3U Compact PCI printed circuit board.
- Qualification of the RTIMS for ground, airborne and space applications.

Accomplishments

- Completed module radiation & environmental tests and analysis
- Successfully designed, built and functionally tested the module
- Added mission flexibility by creating VHDL code that allows RTIMS to reconfigure its memory into a true TMR (Triple Modular Redundant) architecture with 1Gb of storage or into an EDAC (Error Detection And Correction) mode where part of the memory is used to detect and correct errors with 2Gb of storage
- Successfully designed, built and tested the 3U cPCI demo board
- Successfully integrated demo board with flight like computing system
- Capabilities align with Exploration Systems Mission Directorate needs
- 3D Plus intends to commercialize RTIMS

RTIMS Module



Schedule and Deliverables

Schedule:

Phase 1 (18 Months): RTIMS physical module design and development

Phase 2 (6 Months): Complete prototype board for RTIMS module testing

Phase 3 (11 Months): Environmental testing and final analysis

Deliverables:

Monthly Financial Reports, Quarterly Technical Reports, Interim Review, Annual or Final Review, Annual or Final Report, and an Annual Workshop



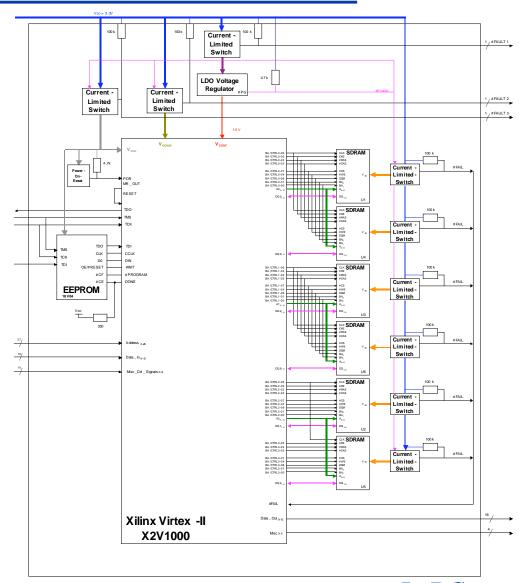


Major Components

- 6 SDRAMs 512Mb
- 1 FPGA Xilinx Virtex II
- 1 EEPROM Xilinx 4Mb
- Current Limiters
- Power Regulator / Power-On-Reset

Interface

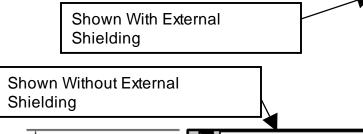
- Single 3.3V Power Supply Required
- External Clock
- 27 Line Address Bus
- 2 Data Busses
 - 16 Line Data In Bus
 - 16 Line Data Out Bus
- Simple SDRAM interface
 - Read/Write with only 4 control signals
 - 2 Status Signals

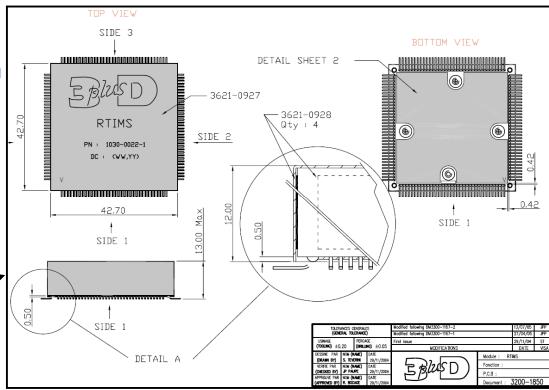


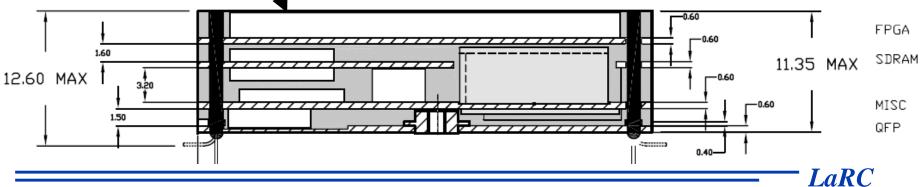


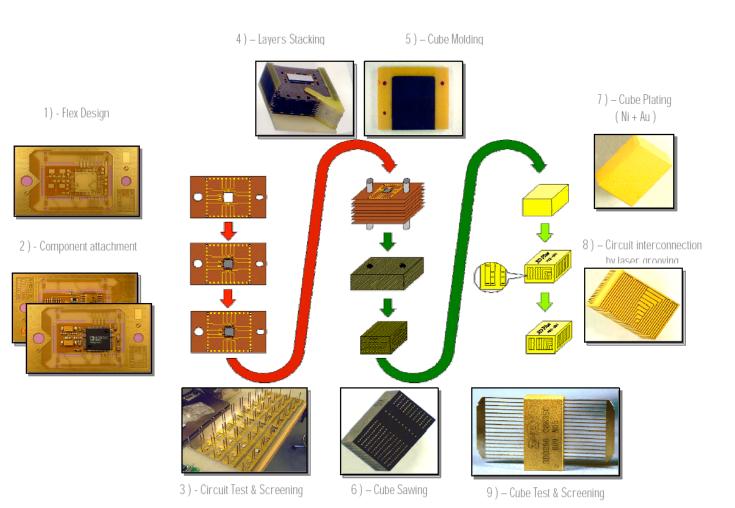


- Dimensions
 - 42.7mmx42.7mmx13mm
- Advanced stacking
 - 3 Active Layers
- QFP 144 Package
- Internal Thermal Drain



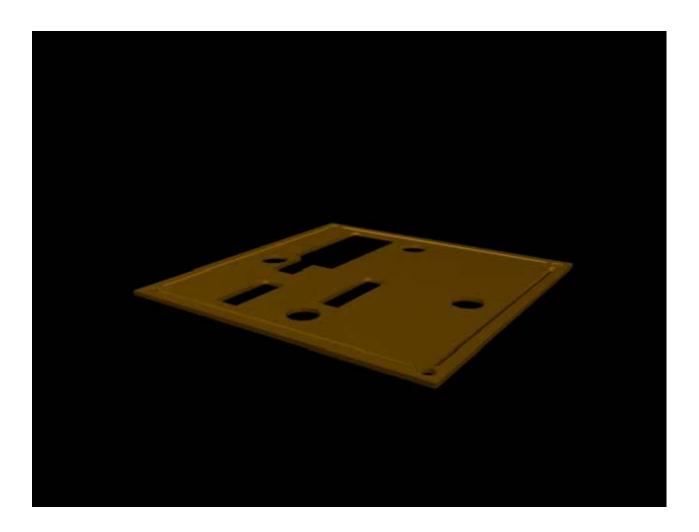






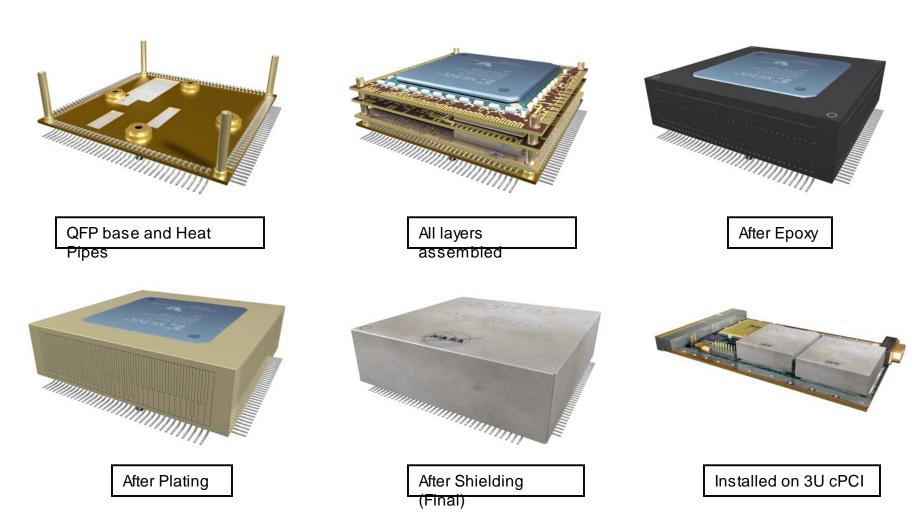


Module Construction Animation





Renderings of RTIMS at several stages of construction





- Component Selection
- Shielding
- Current Limited switches
- Memory Array can be TMR or EDAC (mission dependent)
- FPGA



- A combination of Space, Military and Commercial parts were selected to minimize cost while achieving all goals
- Radiation testing was performed on components without radiation data

			SEL	SEU	TID
Component	Manufacturer	Part Number	(MeV-cm2/mg)	(MeV-cm2/mg)	(Krad (Si))
FPGA	Xilinx	XQ2V1000-4BG575	124	1	200
EEPROM	Xilinx	XQR18V04	120	120	30
SDRAM	Elpida	EDS5108ABTA	80		50
Linear Reg	Texas Instruments	TPS75715	60	N/A	10
Current Limiter	Maxim	MAX893L	N/A	N/A	30
Power on Reset	Maxim	MAX803	N/A	N/A	20

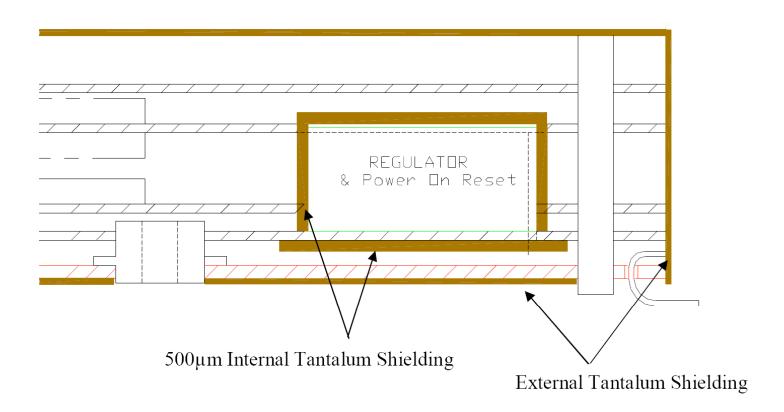
Details in MAPLD 2005 paper: http://www.klabs.org/mapld05/presento/208_ng_p.ppt

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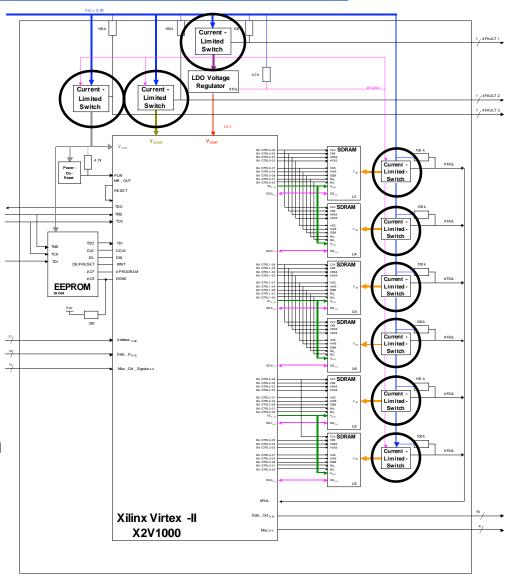
- Tantalum Shielding is employed to increase TID
 - 2 components had low TIDs and required additional shielding





- Prevent Damage from Latch-up Conditions on:
 - Each SDRAM
 - FPGA VCCINT
 - FPGA Vccaux
 - FPGA Vcco, POR & EEPROM
- Sends Failure Signal to the External System

These are used even though each component is latch-up immune for the expected environment providing an extra safety margin



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Two Functional Modes (Mission Dependent)

EDAC Configured SDRAM

- Single bit error correction
- Double bit error detection
- Module memory capacity of 128M x 16 bits (2Gb)
- Multiple data bit errors induced by SEU are not corrected
- Array Scrubbing

TMR Configured SDRAM

- All data bits are triplicated
- Module memory capacity of 64M x 16 bits (1Gb)
- Multiple data bit errors induced by SEU are corrected
- Array Scrubbing

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- FPGA requires redundancy to guarantee correct operation in the presence of one Single Event Upset
- FPGA requires a method of removing Single Event Upsets before more than one accumulates



TMR (Xilinx XTMR Tool)

- Gates utilized
 - Average utilization cost of TMR is ~3.2x
 - RTIMS actual is 4.3x
 - It is closer to 3x for design that is mostly gates
 - It is closer to 6x for design that is mostly flops
 - RTIMS actual: 36% flops
- Internal performance degradation
 - Average performance impact of TMR is ~10%
 - RTIMS actual is ~20%
- I/O performance degradation
 - Non TMR Input Pin
 - Can't lock the FF in the IOB
 - RTIMS actual: increased from 1.8 ns to 3.6 ns
 - Non TMR Output Pin
 - Can't lock the FF in the IOB
 - RTIMS actual: increased from 4.5 ns to 6.4 ns

Details in MAPLD 2005 paper: http://www.klabs.org/mapld05/presento/208_ng_p.ppt

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- Configuration scrubbing
 - Configuration is stored in the RTIMS EEPROM
 - On power up the whole configuration is loaded
 - On scrubbing, only GCLK, CLB, IOB, and memory control are loaded
 - Scrubber logic is TMR and it is part of the FPGA code
 - Scrubbing occurs at programmable intervals
- SelectMap Interface SEFI detection
 - Checks if each configuration scrub was successful
 - Indicates SEFI to system if it wasn't
- Digital Clock Manager
 - Use 3 DCMs for each DCM that is in the original design
 - 3 TMR counters, each counter is clocked by a DCM
 - When one of the counter value is different from the other two, we know which DCM is operating differently than the others

Details in MAPLD 2005 paper: http://www.klabs.org/mapld05/presento/208_ng_p.ppt

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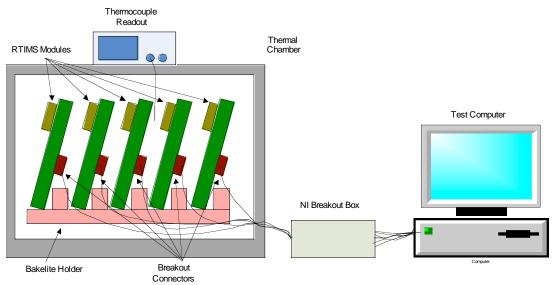
- Life
- Vibration
- Thermal Vac
- Radiation

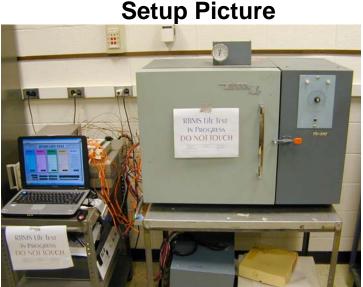


Life Testing

- For this testing we used guidelines established in MIL-STD-883 Method 1005.8
- Chamber is at devices maximum rated temperature of +85°C.
- Devices run at full speed for 1000 hours
- 4 Devices tested and all passed

Setup Diagram



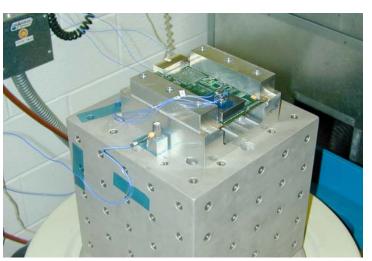




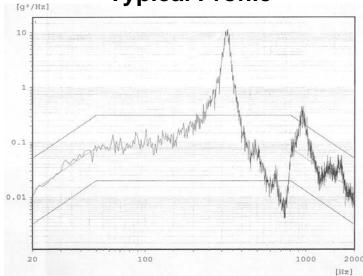
Vibration Testing

- RTIMS Modules were subjected to a base excitation corresponding to GEVS-SE (General Environmental Verification Guidelines for STS & ELV Payloads, Subsystems, and Components) environment for space qualification as dictated in MIL-STD-883 and MIL-STD-202
- The random test spectrum was 10.0 Grms vibration over a frequency range of 20 to 2000 Hz
- 5 articles tested, all passed
- 1 article taken to flight qualification levels (14.1 Grms) and passed

Picture of Setup



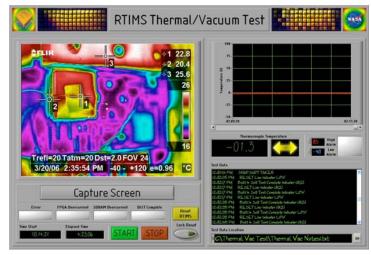






Thermal Vac Testing

- The thermal profile will range from -40°C to +85°C as per MIL-STD-883-F Method 1010.8 and manufacturer's specifications
- Internal pressure will be held at 10⁻⁵ torr or less for the duration of the test. This corresponds to an altitude of greater than 200 km
- 5 articles were tested

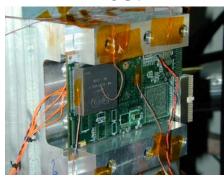


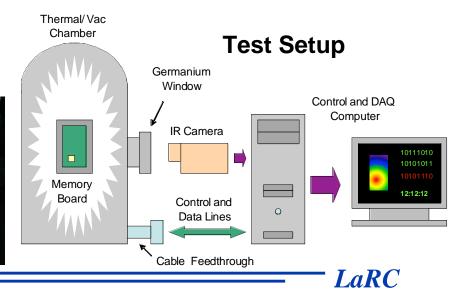
Screen Shot with Thermal Image

Picture of Chamber



Device Under Test





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- Analysis done for a Geosynchronous orbit
- Environments
 - Solar inactive, epoch 2006
 - AE8Min model for Trapped Electrons, AP8Min model for Trapped Protons and a Quiet magnetosphere (i.e. no Solar Protons)
 - Solar active, epoch 2010
 - AE8Max model for Trapped Electrons, AP8Max model for Trapped Protons and the ESP model (using 95% Conf.) for the Solar Protons and a Stormy magnetosphere
- Thin-walled (10, 60, 125 mils of Aluminum) hollow sphere 2 meters in diameter with RTIMS at the center
- NOVICE radiation transport code was used to calculate radiation dose within RTIMS

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RTIMS Survival Times

• 10 mils Vehicle Shielding (Aluminum): 138 Days

• 60 mils Vehicle Shielding (Aluminum): 1.65 Years

•125 mils Vehicle Shielding (Aluminum): 6.67 Years

	Component's Total Dose Limit K rad(si)	10 mils K rad(Si) per year	60 mils K rad(Si) per year	125 mils K rad(Si) per year
Outside RTIMS		12600	440	45
I Limiters	30	21.4	4.95	1.28
Regulator	10	8.0	2.25	0.823
ResetGen	20	7.79	2.2	0.817
SDRAMs	50	12.2	3.14	0.971
EEPROM	R/O: 30; R/W: 10	26.4	6.11	1.5
FPGA	200	29.6	6.47	1.49



RTIMS Survival Times

• 10 mils Vehicle Shielding (Aluminum): 124 Days

• 60 mils Vehicle Shielding (Aluminum): 1.25 Years

•125 mils Vehicle Shielding (Aluminum): 3.61 Years

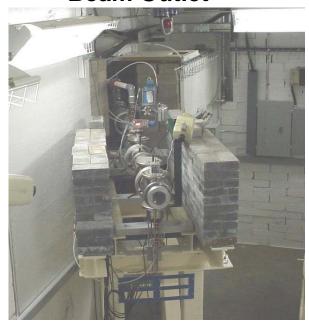
	Component's Total Doze Limit K rad(si)	10 mils K rad(Si) per year	60 mils K rad(Si) per year	125 mils K rad(Si) per year
Outside RTIMS		12700	450	49
I Limiters	30	23.8	6.59	2.38
Regulator	10	9.8	3.55	1.77
ResetGen	20	9.6	3.5	1.76
SDRAMs	50	14.3	4.56	1.97
EEPROM	R/O: 30; R/W: 10	29.3	8.02	2.77
FPGA	200	32	8.17	2.61

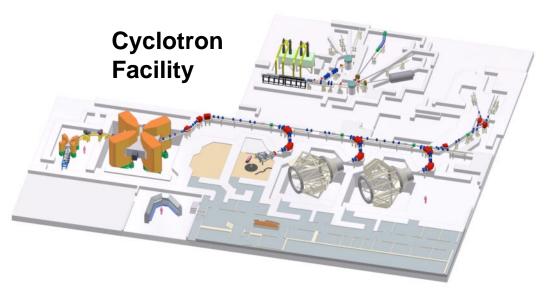
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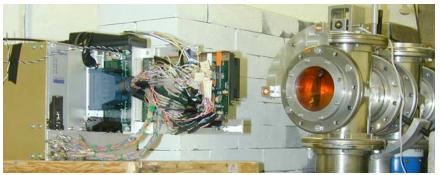
- Indiana University Cyclotron Facility
- Proton Beam
 - Very high energy beam
 - No de-lidding is required

Beam Outlet





Test Setup



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Test Software

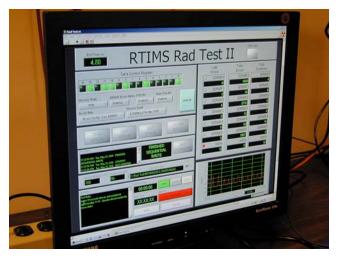
- On RTIMS

- Exercises SDRAM control functions
- Exercises all memory locations
- Tracks & reports data errors
- Reports BIST status

On Test Control PC

- Exercises the RTIMS module interface
- Keeps running totals of data errors
- Controls test sequence
- Logs all events
- Monitors current draw

Software Screen Shot



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- Sensitivity of Xilinx configuration memory tested
 - Average over 6 runs, 2 RTIMS modules
 - Cross section [cm2]: 4.8E-14
 - Consistent with SEE Consortium report on Virtex-II of 3.75E-14



- Test was completed in May 2006
- Error rate is being compiled now



- A SEFI error was defined as the conditions that required an initialization of the FPGA from the EEPROM.
- All errors were recoverable by the reloading of the configuration from the EEPROM
- Test was completed in May 2006
- Error rate is being compiled now



- Total dose
 - Better than target of 100 Krad (Si)
- SEL
 - Better than target 60MeV –cm²/mg
 - None observed during test
- SEU
 - Test was completed in May 2006
 - It is being compiled now



- Trade flux vs test time
- SEU rate of the test environment >>> SEU rate of the operating environment
 - SEU mitigation scheme may be overrun by the rate error
- SEU emulator may be helpful to exercise the mitigation scheme prior to beam testing



Improving the error rate

- Initiate DCM error recovery immediately instead of waiting for the next scheduled time
- Initiate configuration scrubbing when an error is detected instead of waiting for the next scheduled time
- Minimize the use of large fan out nets

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- Validates a set of processes and methods for using "soft" reconfigurable FPGAs in space missions
- Does not require a radiation hardened external "scrubber"
- Provides a flexible memory whose reliability can be adjusted based on the requirements of the mission
- Demonstrates a space ruggedized heterogeneous stacking technology achieving 3-4 times space savings and improved signal integrity



- RTIMS meets or exceeds design requirements
- Manufacture of the RTIMS module complete
- Integration with flight like computing system complete
- Environmental testing nearly complete
- TRL 6 Achieved